WHAT IS CLAIMED IS:

1. A memory device comprising:

at least one memory block requiring a word line pre-charge time to last long enough to program one or more memory cells associated with one or more selected word lines contained therein; and

a monitoring circuit for detecting that each word line has reached a predetermined threshold voltage to enable a predetermined voltage to be supplied to one or more latches associated with the selected word lines.

2. The memory device of claim 1 wherein the monitoring circuit includes at least one memory cell structurally similar to memory cells of the selected word lines.

3. The memory device of claim 1 wherein the monitoring circuit is formed such that it needs the longest word line pre-charge time comparing to all selected word lines.

4. The memory device of claim 1 wherein the monitoring circuit includes at least one word line detection circuit for comparing the word line voltage with the threshold voltage.

5. The memory device of claim 1 wherein an output of the monitoring circuit is tied with a programming triggering signal of the memory device as two inputs to an AND gate for generating an output signal indicating that a programming sequence may proceed.

6. The memory device of claim 1 wherein the monitoring circuit includes two word line detection circuits each being connected to a memory block for detecting

whether the word lines for either even or odd rows of the memory block have surpassed the threshold voltage.

7. A memory device comprising:

at least one memory block requiring a word line pre-charge time to last long enough to program one or more selected memory cells associated with word lines contained therein;

a first monitoring circuit for detecting a first test word line contained therein to reach a predetermined threshold voltage to enable a predetermined voltage to be supplied to a first set of selected memory cells; and

a second monitoring circuit for detecting a second test word line contained therein to reach the predetermined threshold voltage to enable the predetermined voltage to be supplied to a second set of selected memory cells.

8. The memory device of claim 7 wherein the first and second monitoring circuits each includes one or more memory cells structurally similar to memory cells of the first and second set respectively.

9. The memory device of claim 8 wherein the first and second test word lines in the first or second monitoring circuit rise slower in voltage than the word lines associated with the first or second set of selected memory cells respectively when being charged.

10. The memory device of claim 7 wherein the first and second monitoring circuits includes a first and second word line detection circuits respectively for comparing the voltages of the first and second test word lines with the threshold

voltage.

11. The memory device of claim 10 wherein the first and second word line detection circuits each generates an output signal indicating that the selected memory cells can be provided with the predetermined voltage for programming same.

12. A method for controlling a memory device, the memory device having at least one memory block having a plurality of memory cells associated with a plurality of word lines, the method comprising:

providing a first signal initiating a programming cycle;

generating a second signal from a monitoring circuit indicating that a programming sequence can be initiated for one or more selected word lines; and

providing a predetermined high voltage to one or more source lines associated with the selected word lines after recognizing the second signal,

wherein the monitoring circuit contains structurally similar memory cells as those in the selected word lines and has the longest pre-charge time among all.

13. The method of claim 12 further comprising providing a third signal indicating a beginning of imposing the predetermined high voltage.

14. The method of claim 12 wherein the generating further includes detecting whether one or more test word lines in the monitoring circuit have reached a voltage level higher than a predetermined threshold voltage.

15. The method of claim 12 wherein the generating further includes detecting

whether a test word line in the monitoring circuit has reached a voltage level higher than a predetermined threshold voltage to indicate all selected even or odd word lines have reached the voltage level.

16. The method of claim 12 further comprising providing a first operating voltage to the memory cells of the selected word lines prior to the programming sequence.

17. The method of claim 16 further comprising providing a second operating voltage after the pre-charge time.

18. The method of claim 17 wherein the first operating voltage is about 2.5V.

19. The method of claim 17 wherein the second operating voltage is about 1.8V.

20. The method of claim 17 wherein the predetermined high voltage is about 10.5V.